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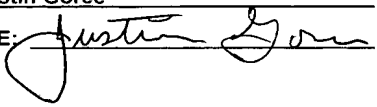
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Serial No. **Not yet assigned**

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For: **IMAGE SENSING STRUCTURE**

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Sir:

     Transmitted herewith is a certified copy of the priority European Application No.03251149.5.

     Respectfully submitted,

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Image sensing structure

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1   <u>Image Sensing Structure</u>

2

3   The present invention relates to an image sensing

4   structure, and in particular but not exclusively to

5   an image sensing structure comprising a photodiode

6   that provides highly accurate matching between

7   pixels.

8

9   Due to tolerances in the manufacturing process of

10   photodiodes used in solid state imaging devices,

11   there is usually a mismatch in sensitivity between

12   pixels. In the case of a camera that takes pictures

13   to be viewed by humans, the tolerances can be

14   relatively low while creating an image of acceptable

15   accuracy. A mismatch of around five percent is

16   acceptable. However, for other applications such as

17   cameras used for machine vision or optical mice, the

18   allowable mismatch is much less, typically around

19   one percent.

20

21   The classical way of ameliorating such a mismatch is

22   to remove it at a system level using calibration and

compensation techniques. However, calibration requires special setup and also storage of the compensation coefficients, while compensation requires real-time processing, costing silicon and consuming power. Hence, both these techniques are complex to perform and are expensive.

As the areas of technology requiring an ameliorated mismatch are areas which are commercially expanding, there is a need for a photodiode structure that provides improved matching between pixels.

According to the present invention there is provided a photodiode as claimed in the attached claims.

The present invention shall now be described, by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 shows a first prior art image sensing structure;

Fig. 2 shows a second prior art image sensing structure;

Fig. 3 shows an image sensing structure in accordance with a first embodiment of the present invention;

Fig. 4 shows an image sensing structure in accordance with a second embodiment of the present invention; and

1

2   Fig. 5 shows an image sensing structure in

3   accordance with a third embodiment of the present

4   invention.

5

6   In transistor fabrication, multiple transistors of

7   similar conductivity types are commonly located in a

8   single well. In normal use, the well is reverse

9   biased with respect to the transistor and the

10   substrate and there is virtually no current flowing

11   into or out of the well and transistor. The

12   transistors therefore do not interact, and so the

13   electrical properties of the well are usually

14   ignored.

15

16   However, the situation with photodetectors is very

17   different. Incident light creates a current that

18   flows into and/or out of the well, and the well's

19   capacitance often determines the photodetector's

20   sensitivity. Thus, the electrical properties of the

21   well are very important to the operation of the

22   detector.

23

24   In a CMOS image sensing structure, the voltage out

25   is governed by the equation:

26

27   Voltage out = (number of photons x quantum

28   efficiency x time x electronic charge) / capacitance

29   of the sense node).

30

31   As the light collection (number of photons),

32   conversion (quantum efficiency) and collection

1 · process is largely the same for all pixels, the

2 variation in the capacitance of the sense node is

3 the main cause of variations in sensitivity.

4

5 These variations are due to manufacturing

6 tolerances, and are fixed for a particular sensor,

7 giving the name "Fixed Pattern Noise" (FPN). As the

8 variation is fixed and not random, it is more

9 accurately called Photo Response Non-Uniformity

10 (PRNU).

11

12 Fig. 1 shows a common form of CMOS image sensing

13 structure. An epitaxial layer 10 is formed on a P

14 substrate 12. A photodiode comprising an N-well

15 collection node 14 with surrounding P-wells 16 is

16 formed in the epitaxial layer 10. The collection

17 node 14 has a conductor 18 attached which carries a

18 signal to a transistor 20, which is part of readout

19 electronics.

20

21 The photodiode illustrated in Fig. 1 is a relatively

22 small photodiode, having a width of less than ten

23 micrometers. Typically, such a photodiode will have

24 a width of between four and six micrometers. As

25 also illustrated in Fig. 1, the epitaxial layer 10

26 has a depth of between four and five μm, and both

27 the N-well and P-wells have a depth of three μm, as

28 measured from the upper surface of the epitaxial

29 layer 10.

30

31 Light 22 impinging on the semiconductor produces

32 electron/hole pairs. There is an electron field

1   around the sense node 14 to attract the electrons

2   there. This electron field is a combination of

3   doping and applied voltage. The position at which

4   electrons e1-e4 are liberated from silicon atoms is

5   a statistical process but is wavelength dependent.

6   For visible light (typical wavelengths from 450nm to

7   650nm) impinging on silicon, the greatest production

8   of electrons occurs at depths from 1 μm to 5μm. To

9   collect as many electrons as possible, a p-n

10   junction should be provided such that that distance

11   the electrons have to diffuse to the junction is

12   minimised. Thus, a p-n junction at around half this

13   depth is optimal. Therefore, N-Well is usually used

14   to form the p-n junction as it occurs at around this

15   depth.

16

17   A problem with this technique is that well

18   implantation is not a critical parameter for CMOS

19   transistors and hence is not particularly well

20   controlled. The width of the collection node 14,

21   shown by X in Fig. 1, varies from part to part and

22   pixel to pixel, by a typical variation dX. The

23   value of dX for the photodiode of Fig. 1 is

24   typically ±300 nm. This variation in the width of

25   the collection node 14 causes variation in the

26   capacitance of the photodiode, leading to the

27   abovementioned problem of mismatch between pixels.

28

29   Fig. 2 shows a modification that can be made to the

30   structure of Fig. 1. Here, an N+ implant is used as

31   the collection node. N+ is used to construct a

32   transistor 26, and its implantation is very well

1   controlled. The part to part and pixel to pixel

2   variation, represented by dX2, in the photodiode of

3   Fig. 2, typically has a value of ±100 nm.

4

5   Although this gives a photodiode with a more

6   repeatable capacitance, its shallower depth means

7   that its quantum efficiency is lower. For example,

8   in Fig. 1, photo-generated electrons e1-e3 are most

9   likely to be attracted to the well and be collected.

10   In contrast, in Fig. 2, only e2 will be sensed, with

11   e1 and e3 being lost into the well for the readout

12   circuitry.

13

14   Fig. 3 shows a first embodiment of the present

15   invention, which provides a deep yet accurate

16   implant.

17

18   Advanced CMOS technologies use a technique called

19   Shallow Trench Isolation (STI) to control accurately

20   the width of (active) N+ or P+ areas. Photo-resist

21   is patterned outside the active areas. Anisotropic

22   etching is used to etch a deep (typically 2μm)

23   trench. This provides a well defined edge for the

24   implants. After implant, polysilicon is deposited

25   inside the trenches.

26

27   The present invention provides STI 30 around the

28   collection node 28 in order to provide better

29   control of the width, X, of the collection node 28.

30   As seen in Fig. 3, the N-well collection node 28 and

31   the surrounding P-wells 16 have a depth of 3 μm

1 below the upper surface of the epitaxial layer 10,

2 and the STI has a depth of 2 μm.

3

4 In a method of manufacture of the photodiode, the

5 STI is formed prior to implantation of the N-well,

6 thus providing a definite border for the p-n

7 junction to increase control of collection node 28

8 width X, with a typical value for dX3 being ±50 nm.

9

10 This technique combines the advantage of a deep N-

11 well for better quantum efficiency with better

12 control of implantation and hence capacitance. As

13 dX3 << dX1 we get much better matching than N-Well

14 implant photodiodes.

15

16 Ideally, the STI would be as deep, or deeper as the

17 N-Well, as the p-n junction below the STI is a

18 diffuse barrier. However, STI is usually formed at

19 a depth of 2μm, as this is all that is required for

20 transistors. In this situation, two thirds of the

21 diode's capacitance is controlled accurately, which

22 represents an improvement over prior art.

23

24 In addition, it is more economical to remain within

25 the standard process flow, rather than producing a

26 new technology which having such an implant.

27

28 Fig. 4 illustrates a second embodiment of the

29 present invention, which is applicable for

30 relatively large photodiodes, having widths equal to

31 or greater than ten micrometers. Typically, large

32 photodiodes will have widths between forty and sixty

1 μm. An N-well collection node 32 is bounded by STI

2 34. To increase sensitivity, the P-well 16 that is

3 shown in Figs. 1-3 is replaced by P-Epi. This means

4 that all the electrons e1-e4 will most likely be

5 collected by the collection node 32.

6

7 The structure of Fig. 4 provides a good solution for

8 photodiodes, but design rule manuals prohibit this

9 implementation for transistor design. Fig. 5 shows

10 a photodiode according to a third embodiment of the

11 present invention. The critical n-p junction is at

12 the N-Well/STI interface and is well controlled.

13 However, the STI 34 of Fig. 4 is extended, so that

14 the STI 38 of Fig. 5 extends over most of the pixel,

15 suppressing P+ and hence avoiding DRC issues.

16

17 This structure obtains good matching, but at the

18 expense in a slight (5%) drop in quantum efficiency.

19

20 Variations and modifications can be made to the

21 above without departing from the scope of the

22 present invention. In particular, it will be

23 apparent that the conductivity types of the various

24 materials discussed could be reversed, for example,

25 a P-well could be formed in an N-substrate rather

26 than having an N-well formed in a P-substrate.

27

CLAIMS

1.   An image sensing structure comprising a photodiode having a first well of a first conductivity type suitable to act as a collection node, and which is formed in a layer of a second conductivity type, wherein at least an upper portion of the first well is bound on at least part of its horizontally circumscribed perimeter by an insulating trench.

2.   The image sensing structure of claim 1, wherein at least an upper portion of the first well is bound on the entirety of its horizontally circumscribed perimeter by an insulating trench.

3.   The image sensing structure of claim 1 or claim 2, wherein the trench is a shallow trench isolation (STI).

4.   The image sensing structure of any preceding claim, wherein the first well comprises an N-well.

5.   The image sensing structure of any preceding claim, wherein the layer of the second conductivity type comprises a P-well.

6.   The image sensing structure of any of claims 1-4, wherein the layer comprises a P-epitaxial layer.

7. The image sensing structure of any of claims 1-4, wherein the trench covers a large portion of the upper surface of the photodiode.

8. The image sensing structure of claim 6 or claim 7, wherein an n-p junction is formed at the interface between the trench and the first well.

9. The image sensing structure of any preceding claim, wherein the photodiode has a width of less than ten micrometers.

10. The image sensing structure of any of claims 1-8, wherein the photodiode has a width equal to or less than ten micrometers.
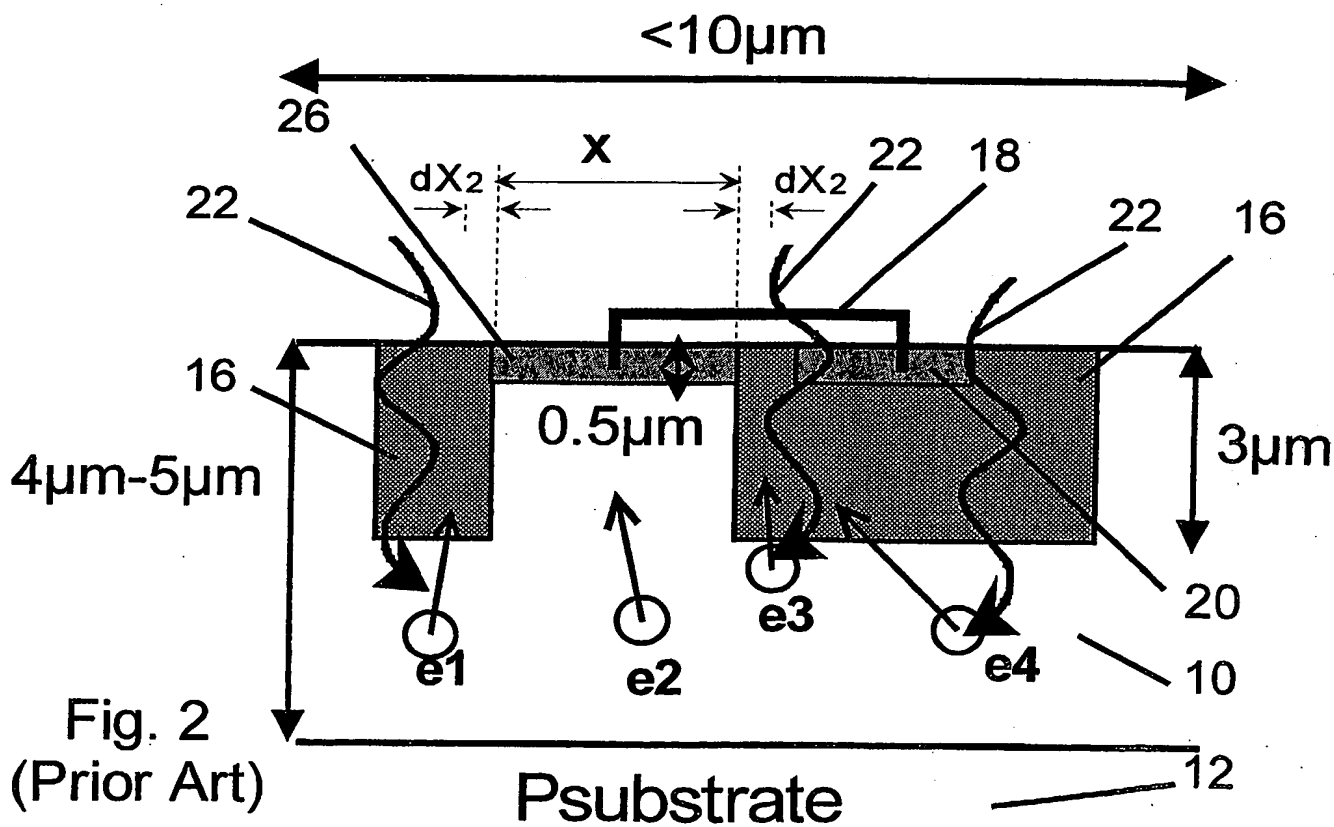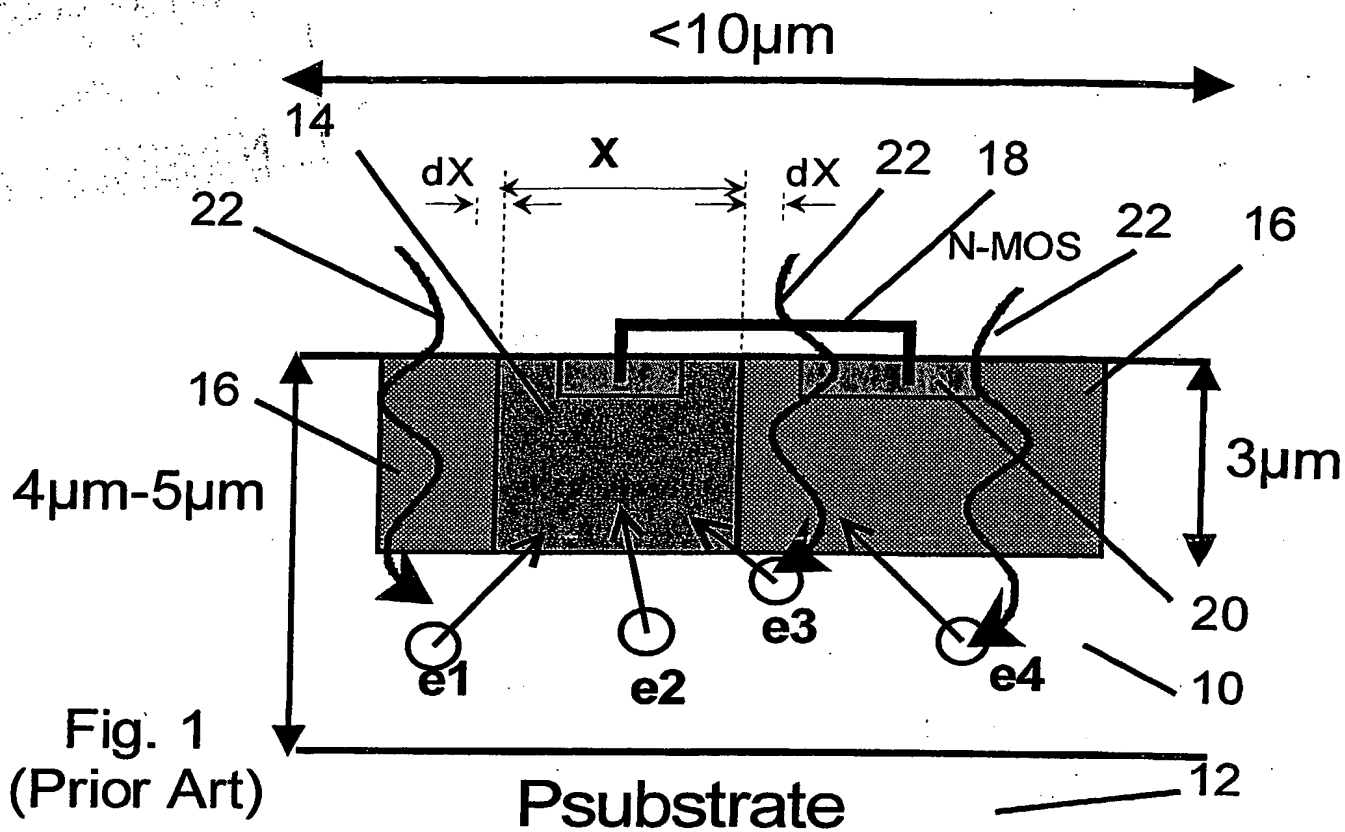
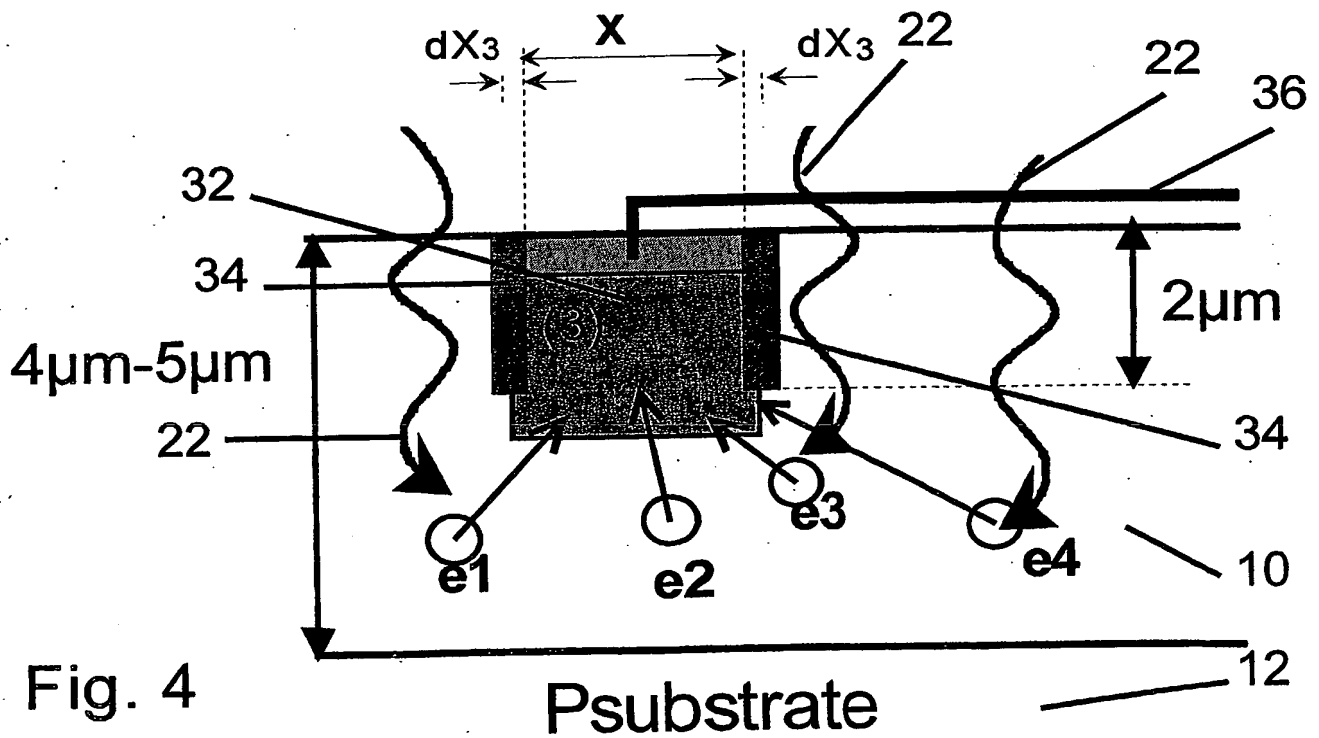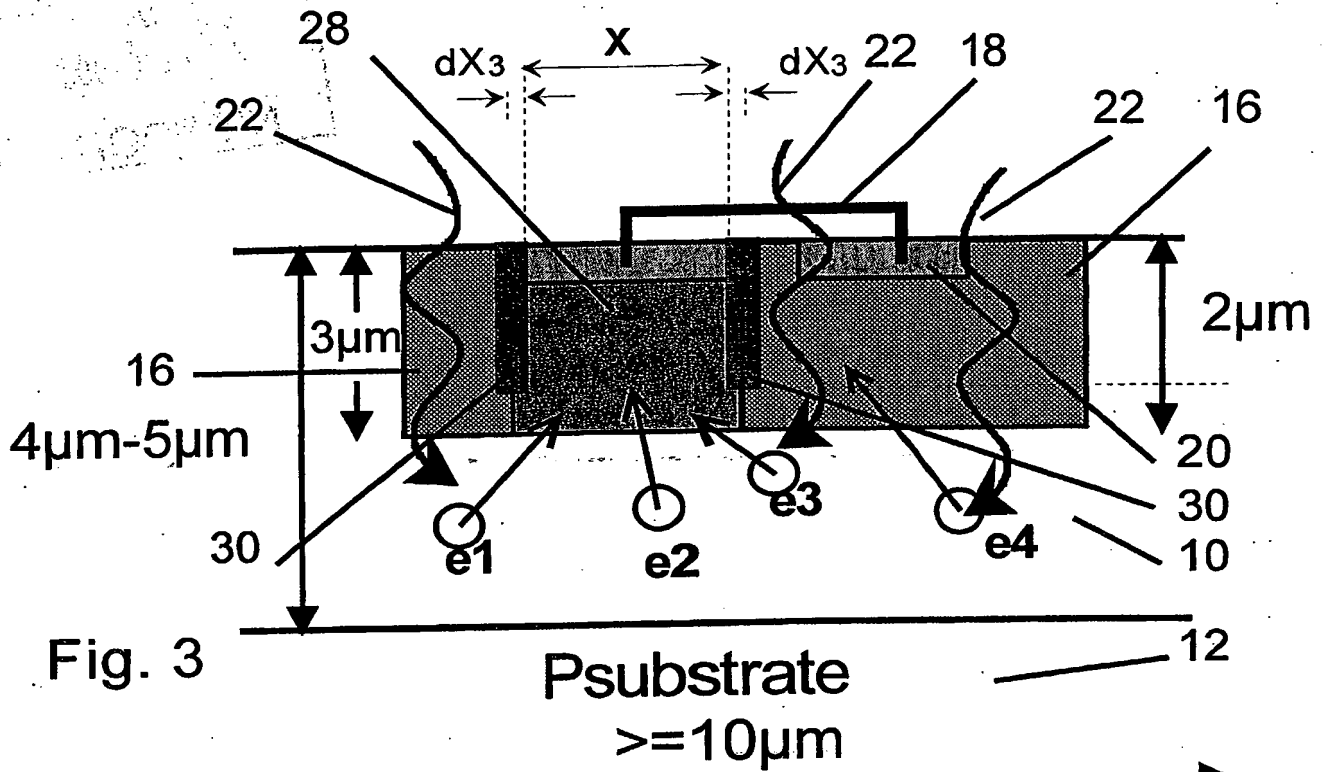1   ABSTRACT

2

3   (Fig. 3)

4

5   A CMOS image sensing structure comprising a

6   photodiode is provided, in which an epitaxial layer

7   (10) is formed on a P substrate (12). The

8   photodiode comprises an N-well collection node (14,

9   26, 28, 32) formed in an epitaxial layer 10. STI

10 (30, 34, 38) is provided around the collection node

11 (14, 26, 28, 32) in order to provide better control

12 of the width, X, of the collection node (14, 26, 28,

13 32). The collection node (14, 26, 28, 32) can be

14 surrounded by P-wells (16) or by epitaxial material

15 (10). It can also be surrounded by epitaxial

16 material (10) with the STI (30, 34) being outwardly

17 extended (38) to ensure compliance with existing
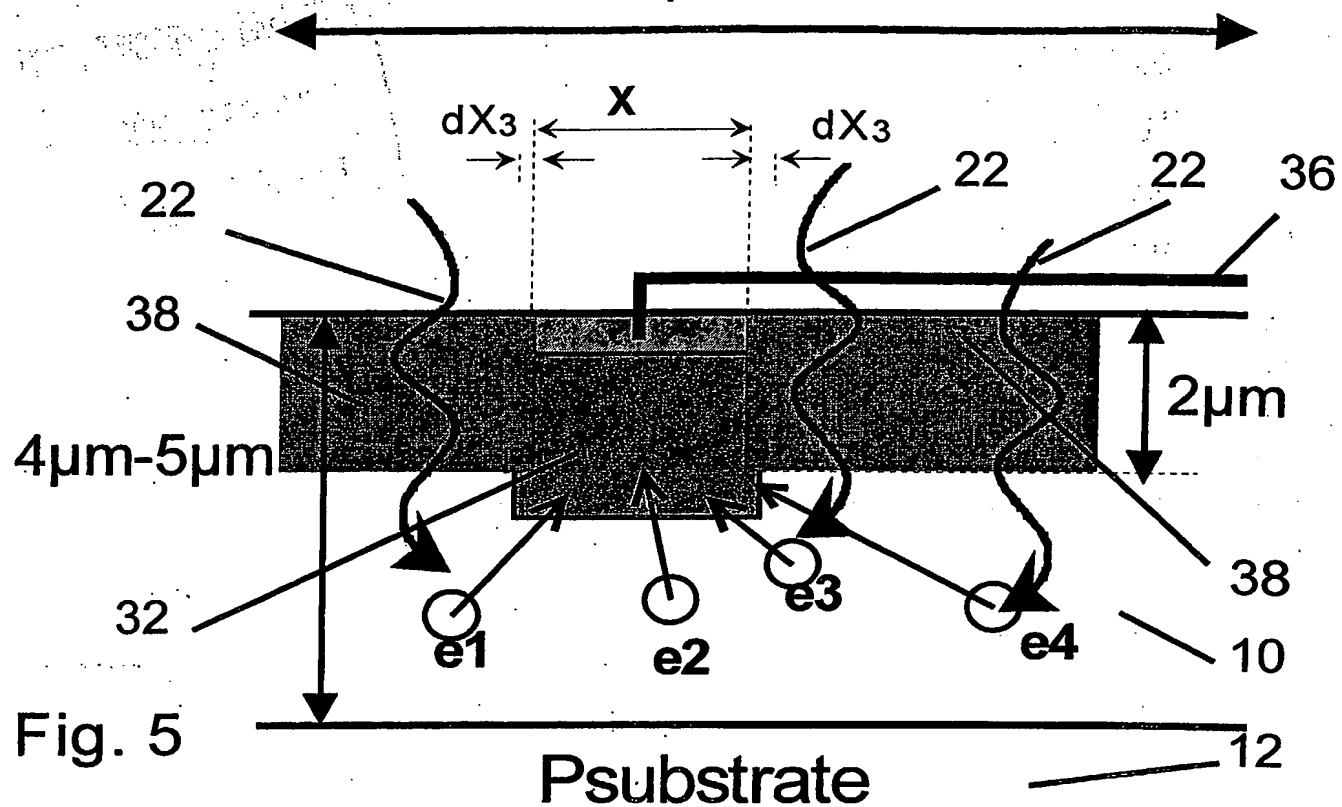
18 design rules.

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<10μm

14

22

X

dX   dX   22   18

N-MOS   22   16

16

4μm-5μm   3μm

20

10

e1   e2   e3   e4

Fig. 1
(Prior Art)   Psubstrate   12

<10μm

26

22

X

dX₂   dX₂   22   18

22   16

16

4μm-5μm   0.5μm   3μm

20

10

e1   e2   e3   e4

Fig. 2
(Prior Art)   Psubstrate   12

Fig. 3

Fig. 4

Fig. 5